L8: Entry 6 of 30 File: USPT Feb 19, 2002

DOCUMENT-IDENTIFIER: US 6349138 B1
TITLE: Method and apparatus for digital transmission incorporating scrambling and forward error correction while preventing bit error spreading associated with descrambling

Detailed Description Text (65):
At the receiver, the two FEC blocks are decoded by passing them sequentially through a single standard FEC decoder thus reducing the cost of a cable modem. Therefore, the FEC utilized with an exemplary embodiment of the present invention is characterized by synchronization within individual subframes and systematic interleaving. Only FEC01340 and FEC11350 are interleaved. Therefore, synchronizing forward error correction and interleaving within a 125 microsecond subframe utilizing an integral number of FEC blocks provides jitter-free STM transmission, since it is not necessary to receive more than a single subframe of transmission at a cable modem before interpretation of FEC code and deinterleaving. Although the parallel FEC description is with respect to two FEC coders, the present invention may also be utilized generally with an interleaving depth of n, requiring n coders. The exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired. The quantity of decoders employed at individual CMs ultimately is a design decision made by the system engineer; balancing the additional cost incurred if each CM were to possess more than one decoder, against the need to mitigate the inherent delay associated with sequential decoding.